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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,080	08/28/2003	Hajime Kimura	12732-162001/ US6582	7214

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FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
NGUYEN, KIMNHUNG T	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/650,080	KIMURA ET AL.	
	Examiner	Art Unit	
	Kimnhung Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/14/066*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-8,11-14 and 16-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-8,11-14 and 16-29* is/are rejected.

7)☒ Claim(s) *30-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/14/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Application has been examined. The claims 3-8, 11-14 and 16-33 are pending. The examination results are as following.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3-5,16-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3 and 16, lines 9-10 and lines 11-12,what is meant by "wherein a connection state between the first and second transistors is switched to one of a series connection states and parallel connection state", because how is the first and second transistors either is switched of a series connection states and parallel connection states.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-8, 11-14 and 16-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stewart et al. (US 5,952,789) in view of Yamagishi et al. (US 6,501,466 cited by Applicant).

Regarding claims 3, 6, 16, Stewart et al. discloses in fig. 5, a current source circuit comprising: a first transistor and a second transistor (T1, T2); and a third transistor (T3, fig. 7), a capacitor element (C2, fig. 5) connected to the gate electrodes of the second transistor (T2); a power source line (see switching power line) connected to one end of the capacitor element (C2); a current source line (fig. 5) connected to the other end of the capacitor element ((C2) because current source connected to the first end (other end) of the first and second capacitors C1, C2, and current source also connected to the transistors T1 and T2); and means for supplying electric charges held in the capacitor element (C1) as current to an object to be driven, and wherein a connection state between the first and second transistors (T1, T2) is switched to parallel connection state

Stewart et al. does not disclose a capacitor element connected to the gate electrodes of the first and the second transistor.

Yamagishi et al. discloses in fig. 1, a capacitor (C) is connected to both the gate electrodes of the first and second transistors (TFT1, TFT2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a one end of the capacitor (C) is connected to both the gate electrodes of the first and second transistors (TFT1, TFT2) as taught by Yamagishi et al. into the system of Stewart et al. for producing the claimed invention because this would provide the picture element drive circuit includes a conversion thin film transistor TF1, where the signal current flows

through the transistor TFT1, and a drive thin film transistor TFT2 for controlling the drive current flowing through a light emitting device consisting of an organic electro-luminescence device (see col. 7, lines 62-67).

Regarding claims 5, 8, 18 Stewart et al. discloses the first and second transistors are an inherent of organic transistors or SOI (because they drive the circuit).

As to claims 4, 7, 17, 20, 23, 25, 27-29, Stewart et al. does not disclose the first, the second and the third transistors are P-channel. Yamagishi et al. discloses in fig. 1, a current source system having the first, the second and the third transistors are P-channel type (see col. 11, lines 19-29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the using of the first, the second and the third transistors are P-channel as taught by Yamagishi et al. into the system of Stewart et al. because this would be selectively injected into the channel in order to shift the threshold voltage toward the enhancement side, which also less expensive to fabricate (see col. 11, lines 23-27).

Regarding claim 11, Stewart et al. discloses in fig. 5, a method for driving a current source circuit having a first transistor (T1), a second transistor (T2), which are connected in parallel, a capacitor element (C1, C2) connected to the gate electrodes of the first transistor and the second transistor and a current source line (fig. 5) and power source line (see switching power line) connected to the capacitor element (C1, C2), the method comprising the steps of: feeding current supplied from the power source line to the power source line; and feeding current

from the power source line to an object to be driven through the first transistor and second transistor (T1, T2), which are connected in series..

Stewart et al. does not disclose the first and second transistors which are connected in parallel.

Yamagis et al. discloses in fig. 1, an active matrix type display apparatus and drive circuit thereof comprising the two transistors TFT1 and TFT2 are connected in parallel.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the two transistors TFT1 and TFT2 are connected in parallel as taught by Yamagis into the system of Stewart et a. for producing the claimed invention because this would provide the picture element drive circuit includes a conversion thin film transistor TF1, where the signal current flows through the transistor TFT1, and a drive thin film transistor TFT2 for controlling the drive current flowing through a light emitting device consisting of an organic electro-luminescence device (see col. 7, lines 62-67).

As to claim 12, claim 12 is similar claim 11 and discussed above.

As to claim 13, Stewart et al. discloses in fig. 5, a method for driving a current source circuit having a first transistor (T1), a second transistor T2), a capacitor element (C2) connected to the gate electrode of the second transistor (T2), a current source line and a power source line (switching power line) connected to the capacitor element (C2), the method comprising the steps of: feeding current to the capacitor element (C2) and holding electric charges such that the capacitor element can feed a predetermined amount of voltage (in the current source, should have the number of voltage such as 8V, fig. 5); supplying current based on the predetermined amount of voltage to the first transistor and second transistor, such that the transistors can feed a

predetermined amount of current (because in the current source also have a number of the current, such as 1 Micro Ampere, fig. 5) ; and supplying the predetermined amount of current to an object to be driven through the first transistor and second transistor, which are connected in series.

Stewart et al. does not disclose the first and second transistors are connected in parallel.

Yamagishi et al. discloses in fig. 1, an active matrix type display apparatus and drive circuit thereof comprising the two transistors TFT1 and TFT2 are connected in parallel.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the two transistors TFT1 and TFT2 are connected in parallel as taught by Yamagish et al. into the system of Stewart et a. for producing the claimed invention because this would provide the picture element drive circuit includes a conversion thin film transistor TF1, where the signal current flows through the transistor TFT1, and a drive thin film transistor TFT2 for controlling the drive current flowing through a light emitting device consisting of an organic electro-luminescence device (see col. 7, lines 62-67).

As to claim14, claim 14 is similar claim 13, and discussed above.

Regarding claims 22 and 26, Stewart et al. discloses in fig. 5 and 7, a current source circuit comprising: a first transistor (T1), a second transistor (T2, fig. 5), and a third transistor (T3, fig. 7) a power source line (see switching power line) connected to one end of the capacitor element (C2 as discussed above); a current source line (fig. 5) connected to the other end of the capacitor element (C2), wherein the capacitor element is connected to the power source line, while the first and second transistors are connected in series when a current is supplied to an element to be driven.

Stewart et al. does not disclose the first and second capacitors are connected in parallel.

Yamagishi et al. discloses in fig. 1, the two transistors TFT1 and TFT2 as discussed above.

Regarding claim 19, Stewart et al. discloses in fig. 5 and 7, a current source circuit comprising: a first transistor (T1), a second transistor (T2, fig. 5), and a third transistor (T3, fig. 7) a power source line (see switching power line) connected to one end of the capacitor element (C2 as discussed above); a current source line (fig. 5) connected to the other end of the capacitor element (C2); and means for supplying electric charges held in the capacitor element (C2) as current to an element to be driven.

Stewart et al. does not disclose that wherein one end of the capacitor element is connected to both the gate electrodes of the first and second transistors.

Yamagishi et al. discloses in fig. 1, a one end of the capacitor (C) is connected to both the gate electrodes of the first and second transistors (TFT1, TFT2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a one end of the capacitor (C) is connected to both the gate electrodes of the first and second transistors (TFT1, TFT2) as taught by Yamagishi et al. into the system of Stewart et al. for producing the claimed invention because this would provide the picture element drive circuit includes a conversion thin film transistor TF1, where the signal current flows through the transistor TFT1, and a drive thin film transistor TFT2 for controlling the drive current flowing through a light emitting device consisting of an organic electro-luminescence device (see col. 7, lines 62-67).

Regarding claims 21, 24 and 28, Stewart et al. discloses the first and second transistors are an inherent of organic transistors (because they drive the circuit).

Allowable Subject Matter

8. Claims 30-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: None of the cited art teaches the method for driving a current source circuit comprising the steps of: dividing a unit frame period corresponding to an synchronizing timing of video signals input to the signal line into m sub frame periods, SF1, SF2... and SFm (where m is a natural number of two or larger) and providing at least one of the sub-frame period SF1, SF2... and SFm with an erasing time; and performing a setting operation n the current source circuit in the erasing time as claims 30-33.

Response To Arguments

10. Applicant's arguments with respect to claims 3-8, 11-14 and 16-33 filed on 12/14/06 have been considered but are not persuasive.

Applicant states that "Stewart discloses a switching power line that is connected to a capacitor and a current source that is connected to transistors T1 and T2, as shown in fig. 5. As noted by the action with regard to claim 11, Stewart does not disclose that the first and second transistors are connected in parallel. See action at page 5, lines 1-2. As such, Stewart does not describe or suggest a current source where a connection state between the first and second

transistors is switched to one of a series connection state and a parallel connection states, as recited by claim 1". Examiner respective disagrees because how is the first and second transistors either is switched of a series connection states and parallel connection states.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimnhung Nguyen whose telephone number is (571) 272-7698. The examiner can normally be reached on MON-FRI, FROM 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimnhung Nguyen

Patent Examiner

March 16, 2007